Evaluation of Sub-threshold Digital Circuits for Wireless Communication Systems

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***Abstract* – Digital circuit designs in sub-threshold region have been studied in recent years. Their works rely on special purpose CMOS cell library with various voltage conditions for the purpose of adjusting circuit delays. This paper proposed modeling analysis for each typical CMOS logic cell to operate at sub-threshold region. Critical-path delays and power dissipation will be analyzed in strong and weak inversion by considering scale factors from typical to sub-threshold voltage conditions. We evaluated wireless circuits in orthogonal frequency division multiplexing (OFDM) communication receiver. The simulation results clearly show that low voltage is not a barrier for large-scale digital circuits.**

I. Introduction

Various methods and techniques have been found, for example, utilization of concurrent / pipeline architecture with low supply voltage for traditional circuits [1]. Design of sub-threshold circuits operating in a weak inversion region achieves ultra low threshold and supply voltages and have been studied in both analog and digital circuits [2]. Analog circuit has been studied and implemented in many areas such as speech signal and image processing [3]. The idea to study sub-threshold operation comes after many researchers done through conventional analysis such as focusing on low power, low voltage, low frequency, and applying in small circuit systems [4], [5].

Studies on energy reduction techniques have been conducted by researchers in the communities of circuit design, system-level design, real-time operating systems, compilers, communication, and networking, among others. Traditionally, systems have been designed to operate at a fixed supply voltage with a fixed clock frequency. Recently, voltage is scaled down to an appropriate level whenever possible. Such variable-voltage systems can achieve extremely low power/energy consumption compared to the standard systems with fixed supply voltage [3]-[6].

The aim of this study is to archive ultra-low power communication circuits operating at high frequency. In this situation, we focus on implementing large scale sub-threshold circuits and need to explore a new design of only using CMOS standard cell library and simplify modeling procedure of sub-threshold circuits. The conventional design does sub-threshold analysis on transistor level or cell library preparation in multiple voltage conditions [7]. This procedure is disadvantageous to make a rough estimate of circuit performance operating at sub-threshold region. We propose scaled modeling to use only typical cell library, which is suitable for large scaled digital circuits such as wireless communication circuits. The proposed methods analyze each CMOS logic cell operating at sub-threshold region in circuit delays and power dissipation and make scaled factors mapping from typical to sub-threshold voltage conditions. This process does not need to make special purpose CMOS library operating at sub-threshold region. The critical path delay is also obtained by scaling factors and used for determining optimal voltage condition satisfying required timing constrains. For practical examples, we have designed wireless circuits of channel equalizer, FIR filter and FFT used in OFDM receiver. These circuits have been reported in power dissipation by adjusting voltage conditions total to satisfy required timing constrains.

II. Device Characteristics in Sub-threshold Region

A sub-threshold CMOS circuit is defined by a standard CMOS circuit operating in a sub-threshold region (weak inversion region). Since a sub-threshold circuit operates in a weak inversion region, device characteristics of sub-threshold circuits are quite different from those in super-threshold circuits that operate in a strong inversion region [4], [8]. Sub-threshold current is the most dominant among all sources of leakages. It is caused by minority carriers drifting across the channel from drain to source due to presence of weak inversion layer when the transistor is operating in cut-off region ($V_{GS} < V_{TH}$). Figure 1 shows a

MOS transistor that operates in cut-off region. In sub-threshold region, a model of power dissipated in a circuit is given by

$$P_{Dynamic} = \alpha C V_{dd}^2 f_{eff} \quad (1)$$

Where α is the activity factor, C is the total switching capacitance of the circuit, V_{dd} is the power supply, and f_{eff} is the clock frequency.

III. Proposed Scaled Modeling

Figure 2 shows modeling process for digital logic design of sub-threshold circuits. The flowchart of Fig. 2(a) is divided into two parts. First part is extracting critical path cell reports from RTL source codes (e.g., Verilog). Second part is analyzing each logic gate in transistor level circuit simulator (e.g., Spice). The circuit simulator uses CMOS models to predict the behavior of a design. The characteristics of typical logic gates are defined by CMOS cell standard behavior. For circuit modeling, it is combination all behavior for circuit evaluation. In the extraction part, RTL description captures the change in design at each clock cycle. The logic synthesis is used for mapping RTL source codes to logic gate level circuits. Then, critical path cell report can be generated by circuit level modeling for references. The advantage of the proposed method is to use only typical CMOS standard cell. Since the proposed method change only values in the critical path report when converting to typical to sub-threshold voltage condition, there is no need to prepare other cell library operating at sub-threshold region. On the other hand, the conventional method illustrated in Fig. 2(b) must prepares multiple conditions in transistor modeling, CMOS cell library, and logic synthesis to verify digital circuits at various V_{dd} conditions. Table 1 summarizes the comparison of conventional and the proposed methods.

IV. Critical Path Delay Analysis

First we extract logic cell delays operating at typical conditions. Each logic cell delay is defined as $T_k(\Theta)$, where k is a cell index in the extracted critical path (consisting of N logic cells) and Θ is a type of logic gate (e.g., OR, AND, etc.). We examine maximum path delay and power dissipation for each logic cell when changing V_{dd} conditions by the transistor level simulator. The scaling factors of $S_k(\Theta,V_{dd})$ mapping from typical to various V_{dd} conditions can be computed by

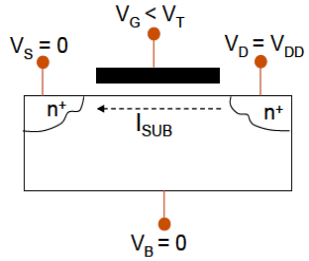

Figure 1: MOS transistor in sub-threshold region

Table 1: Comparing conventional and proposed method.

Preparation for	Conventional	Proposed
CAD Tools	Complex	Simple
Modeling	Long period	Short period
Measurement error	0.1%	0.5%

comparing maximum path delays at each logic cell type. The power function of $P_k(\Theta,V_{dd})$ is also prepared. M is the total number of logic gates in a whole circuit. The total critical path delay for a certain V_{dd} is computed as

$$D_{total}(V_{dd}) = \sum_{k=1}^{N} T_k(\theta) \cdot S_k(\theta, V_{dd}). \quad (2)$$

The total power dissipation is given by

$$P_{total}(V_{dd}) = \sum_{m=1}^{M} P_m(\theta, V_{dd}). \quad (3)$$

In the last step, an appropriate value of Vdd is determined to satisfy required timing constrains and we estimate power dissipation at operating sub-threshold region. In this analysis, we have assigned the load capacitance value at 65Ff for logic gates. We also found that logic gates cannot work correctly when supply voltage is lower than 200mV.

V. OFDM Receiver Architecture

In OFDM receiver, FFT, FIR filter, and channel equalizer are main components except error correcting and roughly determine circuit performance of OFDM demodulator. We focus on FFT, FIR filter and Channel equalizer as example and execute cell logic design in sub-threshold region. Theoretically the channel equalizer can compensate the received data by the inverse of the estimated channel transfer function.

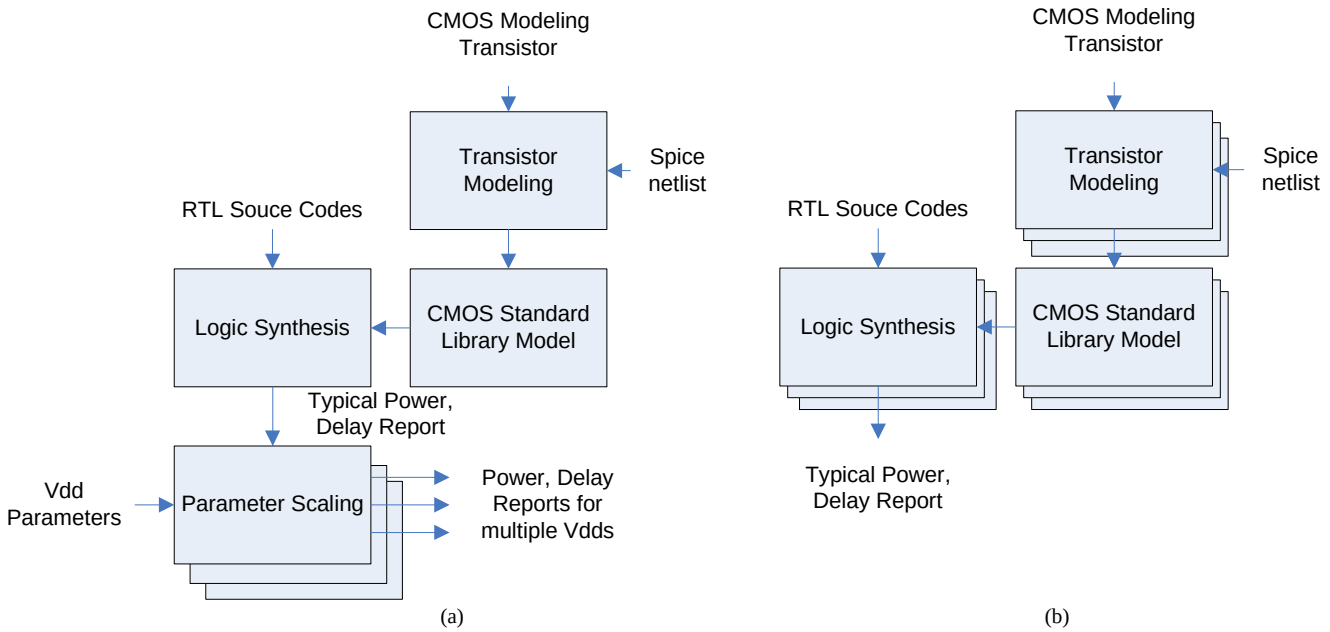

Figure 2: Flowchart for modeling process; (a) proposes method, and (b) conventional method.

VI. Simulation Results

In this section, we have evaluated the OFDM demodulator in power dissipation and critical path delay. The evaluation circuit has been done at 20MHz frequency operation. We have set 4, 6, and 10 bits for bit lengths in channel equalizer, FFT/IFFT, FIR filter. These circuits have been evaluated in power dissipation and critical path delay. The observations for Figure 3 to Figure 6 are summarized in Table 2 to Table 4.

VII. Discussion

We discuss the performance of digital circuit when it operates at different word-length. Table 2 shows the minimum requirement for 4 bits OFDM demodulator to operate in sub-threshold region. The frequency operation is based on IEEE802.11a standard. The nominal voltage operation for 4 bits channel equalizer is 480mV, FIR filter is 560mV and FFT is 580mV. At Table 2, the digital logic circuit can work in sub-threshold region with low voltage supply. Table 3 has shown the 6 bits nominal voltage operation for channel equalizer is 580mV, FIR filter is 730mV and FFT is 650mV. The result indicates that the digital logic circuit can work near the sub-threshold region with low voltage supply. Table 4 shows the minimum requirement for the 10 bits OFDM demodulator
to operate near the sub-threshold region. The nominal voltage operation for 10 bits channel equalizer is 600mV, FIR filter is 760mV and FFT is 680mV. Table 4 has shown that the digital logic circuit for 10 bits has high power dissipation than 6 bits and 4 bits OFDM demodulator. Based on the results of Table 2-4, we can conclude that power dissipation and critical path for digital sub-threshold circuit can be reduce by reducing the bit-length. For example, channel equalizer can operate at sub-threshold when it uses 4 bits length. In this case, channel equalizer can be effective for BPSK modulation system based on bits length. In other cases, 6- and 10- bit digital sub-threshold circuit can be apply to OFDM system for more than 4-QAM (QPSK) modulations with low operating voltage close to sub-threshold voltage.

VIII. Conclusion

We have proposed a method for evaluating large digital circuit for wireless communication which can do analysis in sub-threshold region by using typical CMOS cell library. By using the scaling model, the cost of preparing the different V_{dd} can be eliminated and processing condition is considering reduced. The implementation has been done in OFDM demodulator based on IEEE802.11a standard. Based on the simulation results, the proposed method can do evaluation and shows the power reduction by applying the lowest bits where it can reach to sub-threshold region operation.

References

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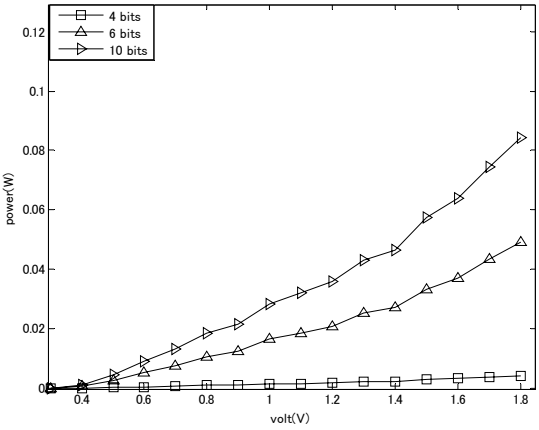

Figure 3: Power dissipation for channel equalizer

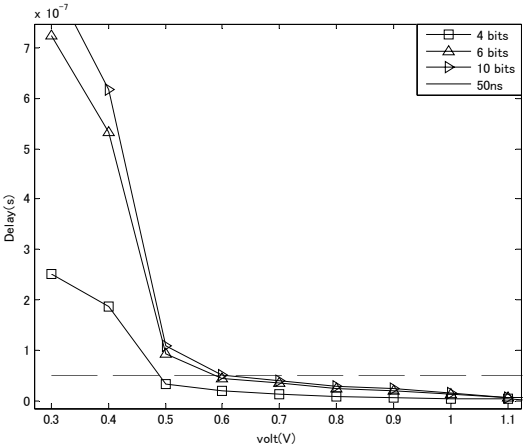

Figure 4: Critical path delay for channel equalizer

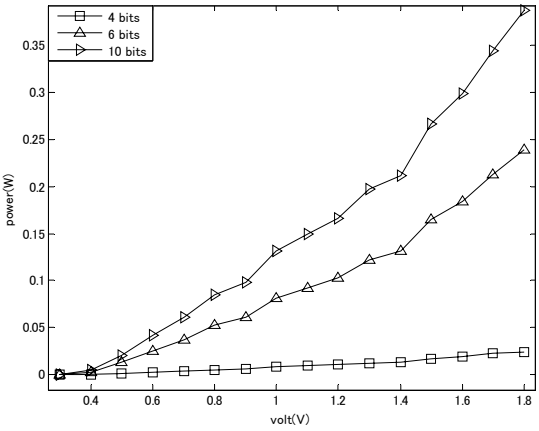

Figure 5: Power dissipation for FIR filter

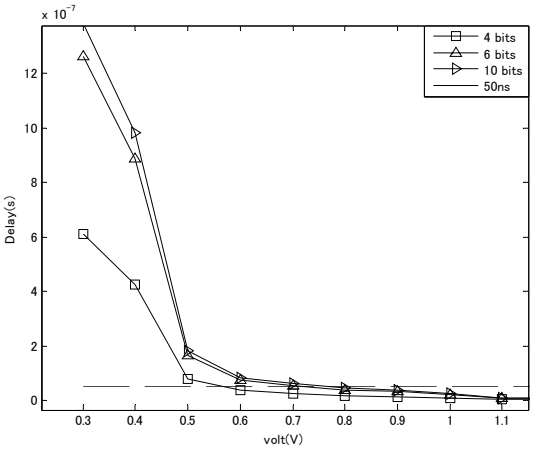

Figure 6: Critical path delay for FIR filter

Table 2: Simulation result for 4 bits FIR, FFT and equalizer

	Equalizer 4 bits	FIR 4 bits	FFT 4 bits
Operating Frequency (MHz)	20	20	20
Logic Gate Counts	234	1,390	5,578
V_{DD} (V)	0.48	0.56	0.58
Power Dissipation (mW)	0.21	2.0	10.0
Power Dissipation (mW) at Typical V_{DD} (1.8V)	2.2	24	98

Table 3: Simulation result for 6 bits FIR, FFT and equalizer

	Equalizer 6 bits	FIR 6 bits	FFT 6 bits
Operating Frequency (MHz)	20	20	20
Logic Gate Counts	1,532	3,222	11,335
V_{DD} (V)	0.58	0.73	0.65
Power Dissipation (mW)	5.0	36	26
Power Dissipation (mW) at Typical V_{DD} (1.8V)	49	238	204

Table 4: Simulation result for 10 bits FIR, FFT and equalizer

	Equalizer 10 bits	FIR 10 bits	FFT 10 bits
Operating Frequency (MHz)	20	20	20
Logic Gate Counts	3,847	14,339	25,542
V_{DD} (V)	0.60	0.76	0.68
Power Dissipation (mW)	9.25	70	53
Power Dissipation (mW) at Typical V_{DD} (1.8V)	84	386	479

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